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A NEW METHOD TO PULSE-TRIGGERED FLIP-FLOP DESIGN WITH ON A SIGNAL FEED-THROUGH SCHEME

S. Dileep Basha ECE Dept., ABIT, Sidhout. dilsal511@gmail.com T. Rama Mohan Reddy Professor ECE Dept., ABIT, Sidhout.

Abstract: During the desktop PC design era, VLSI design efforts have focused primarily on optimizing speed to realize real time functions.

With the growing trend towards portable computing and wireless communication, the need for low power has became as important as performance and area. Since one transistor of the pair is constantly off, the arrangement mix draws huge power just quickly amid exchanging in the middle of on and off states. Therefore CMOS device don't create as much waste heat as different types of logic, for sample TTL or NMOS logic.

CMOS also allow a high thickness of logic function on a chip. It was fundamentally hence that CMOS turned into the most utilized technology to be executed as a part of VLSI technology. CMOS logic dissipates a smaller amount power than NMOS logic circuits because CMOS dissipates power only when switching (“dynamic power”).On a typical ASIC modern 90 Nanometer process, switching the output might take 120picoseconds,and happens once every ten nanoseconds.

---------- 1. INTRODUCTION NMOS logic dissipates power whatever point the transistor is on, on the grounds that there is a present way from Vdd to Vss during the load resistor and the n-type system. Static CMOS gates are extremely control productive on the grounds that they dissipate almost zero power when unmoving.

Prior, the power utilization of CMOS devices was not the significant concern while designing chips, Factor like speed and area subject the design parameters [1]. Dynamic power dissipation is related to the switching activity of the circuit, Here most significant source is charging and discharging of capacitance. The power reduction should be achieved without trading off performance that will make it harder to decrease the leakage during normal operation of the circuitry.

Under the other hand there are several techniques to diminish leakage power. Power gating be the one of such techniques that are well recognized technique where a sleep transistor is added sandwiched between real ground rail and circuit ground. Then these devices are turned off so they will be in the sleep mode to cut off the leakage pathway.

Then it has been given that technique provides a substantial decrease in the leakage the minimal impact on the performance and further peak stage value of ground rebound noise is possible with proposed original technique with improved staggered phase damping technique [2-5]. 2. A NEW METHOD TO PULSE-TRIGGERED FLIP-FLOP DESIGN Flip-Flops (FFs) and latches are the essential storage components utilized broadly as a

part of a wide range of digital designs. Specifically, digital designs these days frequently embrace serious pipelining methods and utilize numerous FF-rich modules.

In the previous decades, numerous works has been committed to enhance the flip's flop's executions. Several flip-flop designs outlines have been proposed to decrease the power and delay. Low power, high speed and area proficient circuit configuration is the real worry in now-a-day VLSI design.

Planning a low power circuit includes a fitting structural engineering of the sequential and combinational circuits utilized as a part of the configuration by utilizing least CMOS logic gates after that using so as to eliminate the excess operations proficient strategies. With a specific end goal to enhance the execution of flip-flop building design and diminish the force utilization broad work has been done in the previous couple of decades. With relentless development in clock frequency and chip limit, power dissipation of the CMOS configuration has been expanding massively.

This outcome in need for advancement of new systems for lessening the power dissipation in VLSI plan. Fast can be accomplished in synchronous systems by utilizing propelled pipelining procedures. In a wide range of digital circuit's flip-flop are utilized as essential storage components. Design styles of flip-flop can be delegated as static and dynamic element.

Static flip-flop are those which can save their stored values regardless of the fact that the clock is ceased. Flip-Flops (FFs) and latches are the essential storage components utilized broadly as a part of a wide range of digital designs. Specifically, digital designs these days frequently embrace serious pipelining methods and utilize numerous FF-rich modules.

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Static flip-flop are those which can save their stored values regardless of the fact that the clock is ceased [6-8]. Basically MOSFET is a four terminal device consisting of source , gate , drain , and bulk terminals, the bulk (or body) of the MOSFET is connected to the high positive or negative terminals depend on type either NMOS or PMOS device now it has a three terminal field effect transistors i.e. only three terminals are appeared at outside.

MOSFET has less leakage current compared to bipolar transistors because of oxide layer present between gate and substrate. NMOSFET consists p type substrate and n type drain and source similarly PMOSFET consists n type substrate and p type drain and source the channel which contain electrons (called NMOSFET or PMOS), or holes (called PMOSFET or PMOS) In the early days metal such as aluminum is used at gate terminal and it has high melting characteristics at high temperatures it is replaced by poly silicon. Poly silicon became dominant, due to its capability to form self-aligned gate.

Metallic gates are achieving high popularity, because without metallic gates it is impossible to increase speed of operation. The symbol of MOSFET contains a line for source channel terminal and drain terminals which are entering orthogonally. The variation between enhancement and depletion mode is shown by a thin line and solid line between terminals.

The insulation provides very high input impedance compared to JFET.MOSFET is a square law device and its output current is proportional to square current Ids. It have special qualities such has high immune radiation, current controlled voltage device and also have more sensitive to electrostatic discharge. MOSFET operation MOSFET operated in two modes either enhancement mode or depletion mode.

In the enhancement mode the channel is not physically present between source and drain. Here we can interchange the drain and source terminals due to its uniform doping characteristics. The basic operation of a MOSFET is as follows. Depend on gate to source voltage charge carriers are accumulating below the gate oxide layer.

The voltage of Vgs at which channel forms is known as threshold voltage and by

controlling drain to source voltage operate the device in desired region. It is operated in two regions i.e. linear region and saturated region in linear region the current increases as voltage applied between drain and source and in saturated region the current becomes constant. By increasing the drain voltage more and more channel gets pinched off and it is known as pinch off voltage.

The increase in source to body voltage increases the threshold voltage then increases the amount of power dissipation and this affect is known as body affect. To avoid this affect source terminal is short circuited to body or substrate. Energy band diagram of MOSFET A known deficiency is it has limited load driving capacities of MOS transistors.

This is due to current sourcing and current sinking abilities associated with P and N transistors. These affect nullified by using super buffers. For gate voltages below the threshold value, the channel has very less amount of carriers, and just a small sub-threshold leakage current can flows through the terminals. Transistors having short channel lengths also experience reduced output impedance because the depletion region variations occurred at drain side have a proportional effect on drain current.

One more important short channel affect is due to hot carriers and due these high velocity carriers the extra electron hole pairs cause flow of current between source and substrate. Finally it is noticed that short channel transistors have larger sub threshold currents than large length channel devices. Intel started creation of a procedure highlighting a 32 nm highlight size (with the channel being much shorter) in late 2009.

The semiconductor business drastically developed and the ITRS, which sets the great support for MOSFET advancement. Verifiably, the troubles with diminishing the measure of the MOSFET have been connected with the semiconductor device manufacture process, the need to utilize low voltages, and with poorer electrical execution requiring circuit update and development whereas the littler MOSFETs are attractive for a few reasons.

The primary motivation to make transistors littler is to pack more devices in a given chip territory. The outcomes in a chip with the same usefulness in a littler range, or chips with more usefulness in the same zone. Since creation costs for a semiconductor wafer are moderately altered, the expense per incorporated circuits is mostly identified with the quantity of chips that can be created per wafer. Subsequently, littler ICs permit more chips per wafer, diminishing the value per chip.

To look after execution, the threshold voltage of the MOSFET must be reduced. As threshold voltage is diminished, the transistor can't be changed from complete turn-off

to complete turn-on with the constrained voltage swing accessible; the circuit outline is a compromise between solid current during the conducting case and low current in the non-conducting case.

The application figures out if to support one over the other. Sub threshold spillage (counting sub edge conduction, entryway oxide spillage and opposite one-sided intersection spillage), which was overlooked before, now can expend upwards of a large portion of the aggregate force utilization of present day elite VLSI chips.

The gate oxide which acts as insulator between the gate and channel ought to be made as small as would be prudent to build the channel conductivity and execution when the transistor is on and to lessen sub-threshold spillage when the transistor is off. Be that as it may, with current gate oxides having a thickness of nearly 1.2

nm (which silicon is ~5 molecules thick) the quantum mechanical wonder of electron tunneling happens between the entryway and channel, prompting expanded force utilization. Innovation highlight size and limit voltage have been scaling for quite a long time for accomplishing high thickness and superior. In light of this innovation pattern, transistor leakage force has expanded exponentially.

As the component size gets to be littler, shorter divert lengths bring about expanded sub-edge leakage current through a transistor when it is off. Low edge voltage additionally brings about expanded sub-limit leakage current on the grounds that transistors can't be killed totally. Hence, static force utilization, i.e., leakage power dissemination, has turn into a critical bit of aggregate force utilization for present and future silicon innovations.

There are a few VLSI procedures to lessen leakage power. Every strategy gives an effective approach to diminish leakage power; however impediments of every system constrain the utilization of every procedure. We propose another methodology, therefore giving another decision to low-leakage power VLSI creators.

The most well-known conventional methodology is the rest methodology .In the sleep approach, both (i) an extra "sleep" PMOS transistor will be put between Vdd and the pull up system of a circuit and (ii) an extra rest NMOS transistor is set between the pull down system and GND. These sleep transistors kill the circuit by removing the force rails.

By removing the force source, this strategy can lessen leakage control viably. Notwithstanding, the strategy brings about decimation of state in addition to a gliding output voltage in sleep mode. 3. SIMULATION RESULTS SIMULATION OF EP-DCO: Fig 1:

The voltage Vs time characteristics of ep-DCOFF D_Q DELAY / Fig 2: The D-Q delay of ep-DCOFF SIMULATION OF MHLFF: / Fig 3 The voltage Vs time characteristics of MHLFF D_Q delay / Fig 4: The D-Q delay of MHLFF SIMULATION PARAMETER OF PROPOSED P-FF: / Fig 5: The voltage Vs time characteristics of PDFF Table 1: Performance Comparison for various Flip-flop (90nm technology) Flip-flop _ Number of transistors _ Total power (µw) _ Minimum D_Q Dealy (ps) _ PDP (femto joule) _ _ ep-DCO _ 28 _ 3.68 _ 6.92 _ 25.46 _ _ MHLFF _ 19 _ 1.12 _ 191.7 _ 214.70 _ _ PDFF _ 14 _ 1.05 _ 2.38 _ 2.49 _ _ _ _ _ _ _ _ _ _4.

CONCLUSION In this Work, a low power Pulse- triggered flip flop embedded logic modules been proposed. An investigation of the overlap phase necessary to go for proper pulse width was provide in arrange just before make the design process simple. The proposed Pulse- triggered flip flop removes the redundant power dissipation present in the modified Hybrid latch flip flop.

A relationship of the future Flip-Flop with the usual Flip-Flops showed that it exhibit lower power dissipation alongside with as good as speed performances. The obtainable embedded logic module performs the Pulse- triggered flip flop in the clock driving power and in internal power dissipation. The reduction in power more or less 70% was observed when basic functions were fixed design.

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